REMARKS

Responsive to the rejection under 35 U.S.C. § 112, first paragraph, claims 1, 2 and 4 have been amended to delete "distinct from the printed wiring substrate". Withdrawal of the foregoing rejection is respectfully requested.

Additionally, claims 1, 2 and 4 have been amended to delete "projecting beyond the planar surface of the printed wiring substrate", for the reason that the Examiner did not consider this recitation to distinguish over the applied prior art.

Claims 1-13 and 16-18 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,218,729 to Zavrel, Jr. et al. The grounds for rejection remain the same as set forth in the previous Office Action.

In response to the remarks portion of the Amendment Under 37 C.F.R. § 1.116 filed December 10, 2001, the Examiner maintained that terminals 810 and 812 are part of capacitor 804 (of Fig. 8 of Zavrel), and therefore within the scope of the claimed capacitor terminals. The Examiner further considered that the capacitor 804 of Zavrel is directly connected to the IC chip 820 through solder bump 828.

Applicants traverse, and request the Examiner to reconsider for the following reasons.

First, Applicants respectively submit that the Examiner has neglected dispositive claim language which patentably distinguishes over the applied prior art.

Namely, as required by the claims, the printed wiring substrate comprises a capacitor accommodation cavity for accommodating the capacitor. The Examiner's position is incorrect in that capacitor plates 860 and 862 of Zavrel are embedded in the laminated substrate 822 and a capacitor accommodation cavity is not disclosed. Rather, as described by Zavrel, the substrate

has a laminated structure of interconnects, where passive devices (such as capacitor 804) are designed into the metal interconnect layers (column 2, lines 2-8). Zavrel et al goes on to further describe the method of fabricating the substrate at column 2, lines 20-22:

> A method of fabricating the substrate of the present invention includes depositing insulative layers and metal layers. Each metal layer is patterned and treated to a photoresist etch step. The patterning includes defining the traces which constitute the interconnects. The structures which constitute the passives are patterned at the same time as the interconnects.

That is, the passive components including capacitor 804 in Zavrel are fashioned by selectively etching the metal interconnect layers in the laminated structure. This is not a description of a capacitor accommodation cavity for receiving a capacitor. Rather, capacitor plates 860 and 862 in Zavrel are embedded in the laminated substrate.

This is further described in claim 1 of Zavrel:

> ..., said substrate including alternating layers of metal interconnects and insulative material, said die having electrical connections to one or more layers of metal interconnects; a tank circuit including an inductor and a capacitor fully constructed from one or more layers of metal interconnects within said substrate,...

Thus, Zavrel does not disclose a capacitor accommodation cavity as required by the present claims.

The significance of the claimed capacitor accommodation cavity for accommodating the capacitor is discussed bridging pages 15-16 of the specification. Particularly, by employing the capacitor accommodation cavity, the capacitor terminals and the substrate terminals are densely located on and around the capacitor. Therefore, the planar size of the IC chip to be connected to the terminals can be made as small as possible, thereby preventing a problem in which the planar size cannot be reduced due to arrangement of the terminals.

For the above reasons, it is respectfully submitted that the present claims are patentable over Zavrel et al, and withdrawal of the foregoing rejection is respectfully requested.

Withdrawal of all rejections and allowance of claims 1-13 and 16-18 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Thrice amended) A printed wiring substrate having a planar surface and a built-in capacitor [distinct from the printed wiring substrate] on which an IC chip is mounted, said printed wiring substrate comprising a capacitor accommodation cavity for accommodating the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals [projecting beyond the planar surface of the printed wiring substrate], wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip comprises a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively flip-chip-bonded directly to a plurality of connection-to-capacitor terminals of the IC chip; and

the plurality of substrate terminals of the printed wiring substrate are respectively flip-chip-bonded to a plurality of connection-to-substrate terminals of the IC chip.

2. (Thrice amended) A printed wiring substrate having a planar surface and a built-in capacitor [distinct from the printed wiring substrate] on which an IC-chip-carrying

printed wiring substrate is mounted, said printed wiring substrate comprising a capacitor accommodation cavity for accommodating the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals [projecting beyond the planar surface of the printed wiring substrate], wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode groups;

the printed wiring substrate comprises a plurality of substrate terminals;

the IC chip-carrying printed wiring circuit comprises a plurality of connection-to capacitor terminals and a plurality of connection-to-substrate terminals;

the plurality of capacitor terminals of the capacitor are respectively bonded in a connection-face-to-connection-face manner directly to a plurality of connection-to-capacitor terminals of the IC-chip-carrying printed wiring substrate; and

the plurality of substrate terminals of the printed wiring substrate are respectively bonded in a connection-face-to-connection-face manner to a plurality of connection-to-substrate terminals of the IC-chip-carrying printed wiring substrate.

4. (Thrice amended) A printed wiring substrate having a planar surface and a built-in capacitor [distinct from the printed wiring substrate] for mounting an IC chip or IC-chip-carrying printed wiring substrate having a plurality of connection-to-capacitor terminals and a plurality of connection-to-substrate terminals, said printed wiring substrate comprising a capacitor accommodation cavity for accommodating the capacitor, characterized in that:

the capacitor comprises:

a pair of electrodes or electrode groups; and

the capacitor comprises a plurality of capacitor terminals [projecting beyond the planar surface of the printed wiring substrate] capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner to a plurality of connection-to-capacitor terminals of the IC chip or IC-chip-carrying printed wiring substrate, wherein the respective capacitor terminals are electrically connected to one or the other of the paired electrodes or electrode group; and

the printed wiring substrate comprises a plurality of substrate terminals capable of being respectively flip-chip-bonded or bonded in a connection-face-to-connection-face manner directly to a plurality of connection-to-substrate terminals of the IC chip or IC-chip-carrying printed wiring substrate.